Figure 7 is a block diagram of a single-chip configuration.

Please replace the paragraph beginning at page 9, line 29 with the following paragraph:

As seen in figure 7, such a single chip codec 108, when combined with a common memory 106, may be used to implement a time-shifted system 100 that can handle both incoming compressed and incoming uncompressed video signals 104, 102. Memory 106 serves the functions of both of the buffers 80, 88 of figure 6. The resulting digital video output 111 is controlled by the host controller to be either real-time or time-shifted as needed.